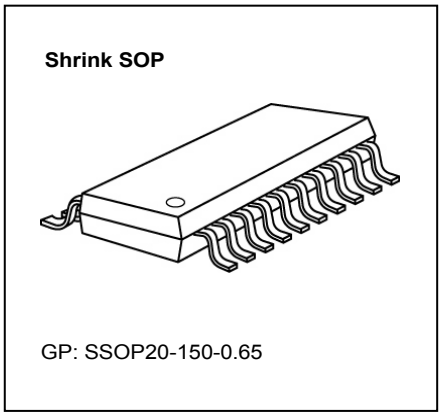
3-Channel Constant-Current Sink Driver for RGB LED Clusters

Features



- 3 constant-current channels for RGB each
- Output current invariant to load voltage change
- Maximum output current per channel: 60mA
- Range of constant current per channel: 5~ 60mA
- Cascading buffers for wired transmission
- Self synchronized signal timing of clock (CLK) and data (SDO)
- Low power consumption: 120mW
- Output current deviation:
  between channels: < ±5% (max.), and
  between ICs: < ±5% (max.)
- Sustaining voltage: 17V
- Built-in voltage regulator working with supply voltage ranging from 6.0V to 12V
- 5 MHz clock frequency at 2-meter cable transmission
- Package type: SSOP20, “Pb-free & Green” package

Applications

RGB LED clusters which are used in:

- Channel letters
- Landscape lighting
- Neon lamp alternative

General Description

MBI6010 is a 3-channel constant-current sink driver for RGB LED cluster, which can be networked to a master controller for scheduled or manual dimming and color control. Each MBI6010 enhances the transmission buffers for data (SDI, SDO), clock (CLK, CLK_OUT), latch (LE, LE_OUT), and output enable (OE, OE_OUT) in a cascading system by the unique “self synchronized signal timing” technology. At MBI6010 output stage, three regulated current ports are adjustable with three corresponding external resistors to match RGB color characteristics. With built-in voltage regulator, MBI6010 provides users with great supply voltage range form 6.0V to 12V, maintains constant current up from 5mA to 60mA and saves the space in a compact cluster. In addition, MBI6010 sustains 17V at output ports. This provides enhanced LED controllability and better mixed-color lighting solution.

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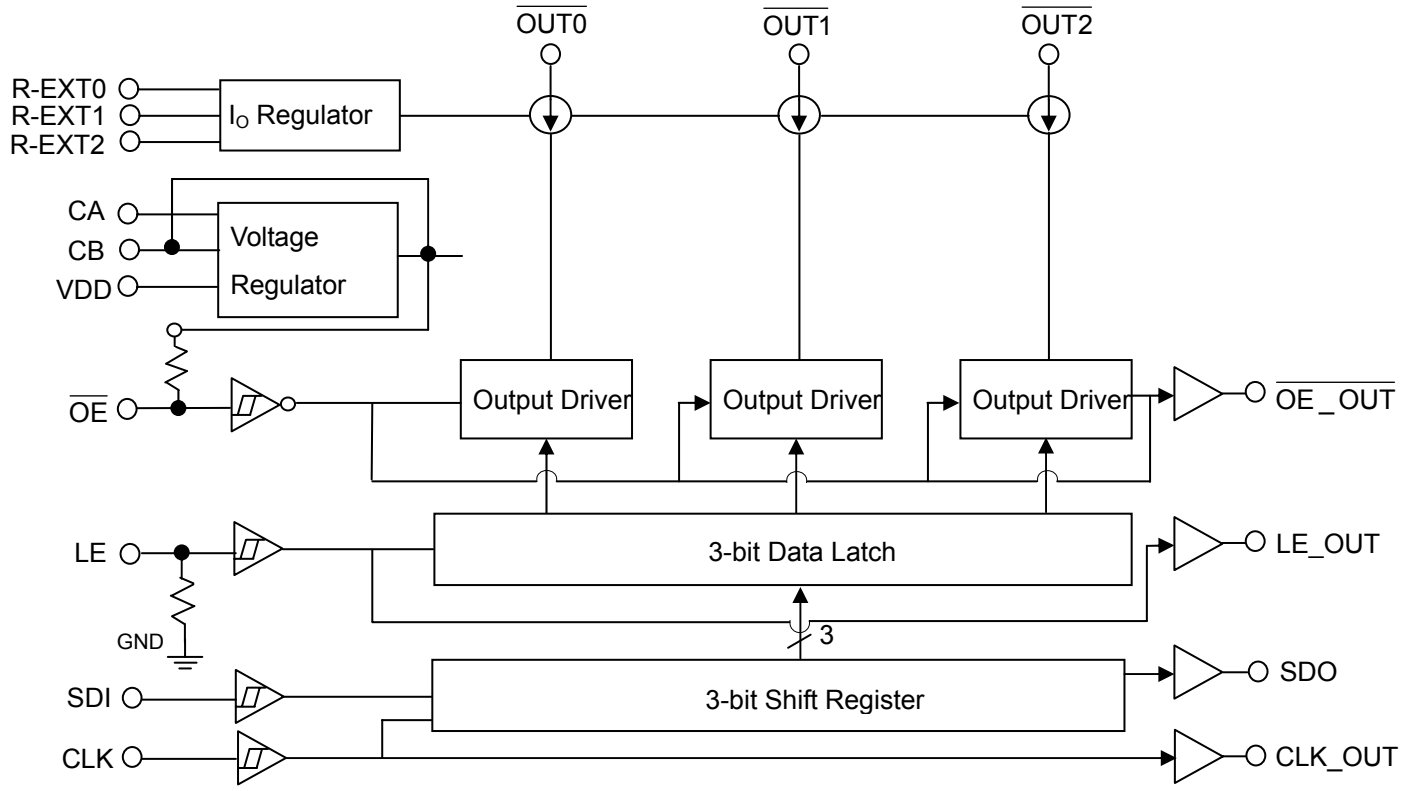
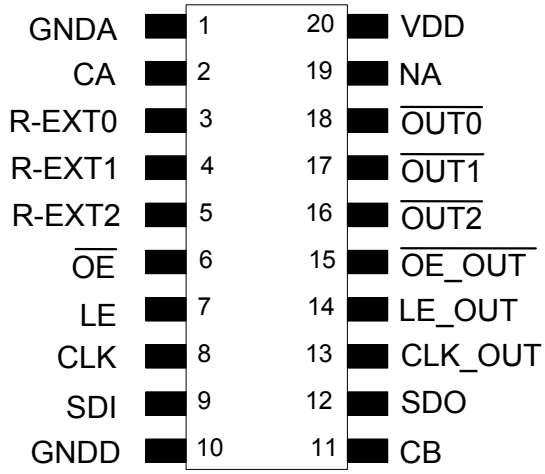
Functional Diagram



Pin Configuration

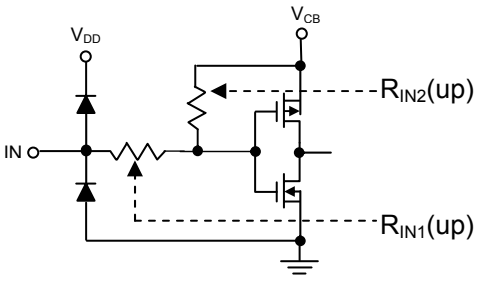


Terminal Description

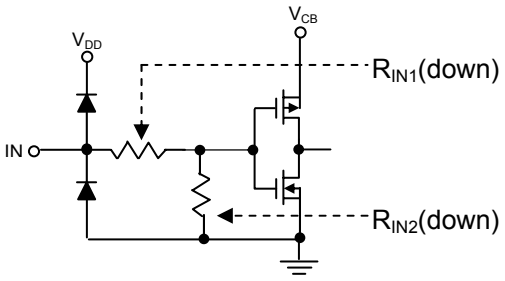
Pin No.	Pin Name	Function
1	GNDA	Analog ground
2	CA	Connected to a compensated capacitor for the regulator output.
3,4,5	R-EXT0,1,2	Input terminal used to connect an external resistor for setting up output current for all output channels
6	$\overline{OE}$	Output enable input terminal When $\overline{OE}$ is active (low), the output ports are enabled; when $\overline{OE}$ is inactive (high), all output ports are turned off (blanked)
7	LE	Data strobe input terminal The data in shift register is transferred to the data latch when LE is high. The data is latched when LE goes low.
8	CLK	Clock input terminal for data shift on rising edge
9	SDI	Serial data input terminal to the shift register
10	GNDD	Digital ground
11	CB	Connected to a compensated capacitor for the regulator output.
12	SDO	Serial data output terminal to be connected to the SDI of the next driver IC. SDO signal changes on falling edge of CLK.
13	CLK_OUT	Clock output terminal, CLK replica, connected to the next CLK
14	LE_OUT	LE output terminal, LE replica, connected to the next LE
15	$\overline{OE}\_OUT$	$\overline{OE}$ output terminal, $\overline{OE}$ replica, connected to the next $\overline{OE}$
16,17,18	OUT0,1,2	Constant current output terminal
19	NA	Not used
20	VDD	Supply voltage terminal

Equivalent Circuits of Input and Output Terminals

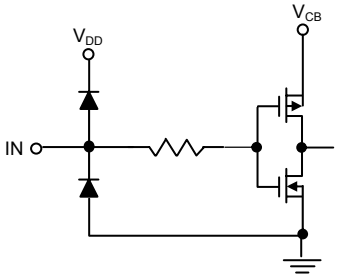
$\overline{OE}$ terminal



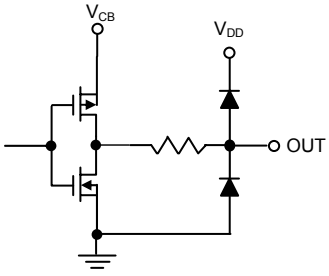
LE terminal



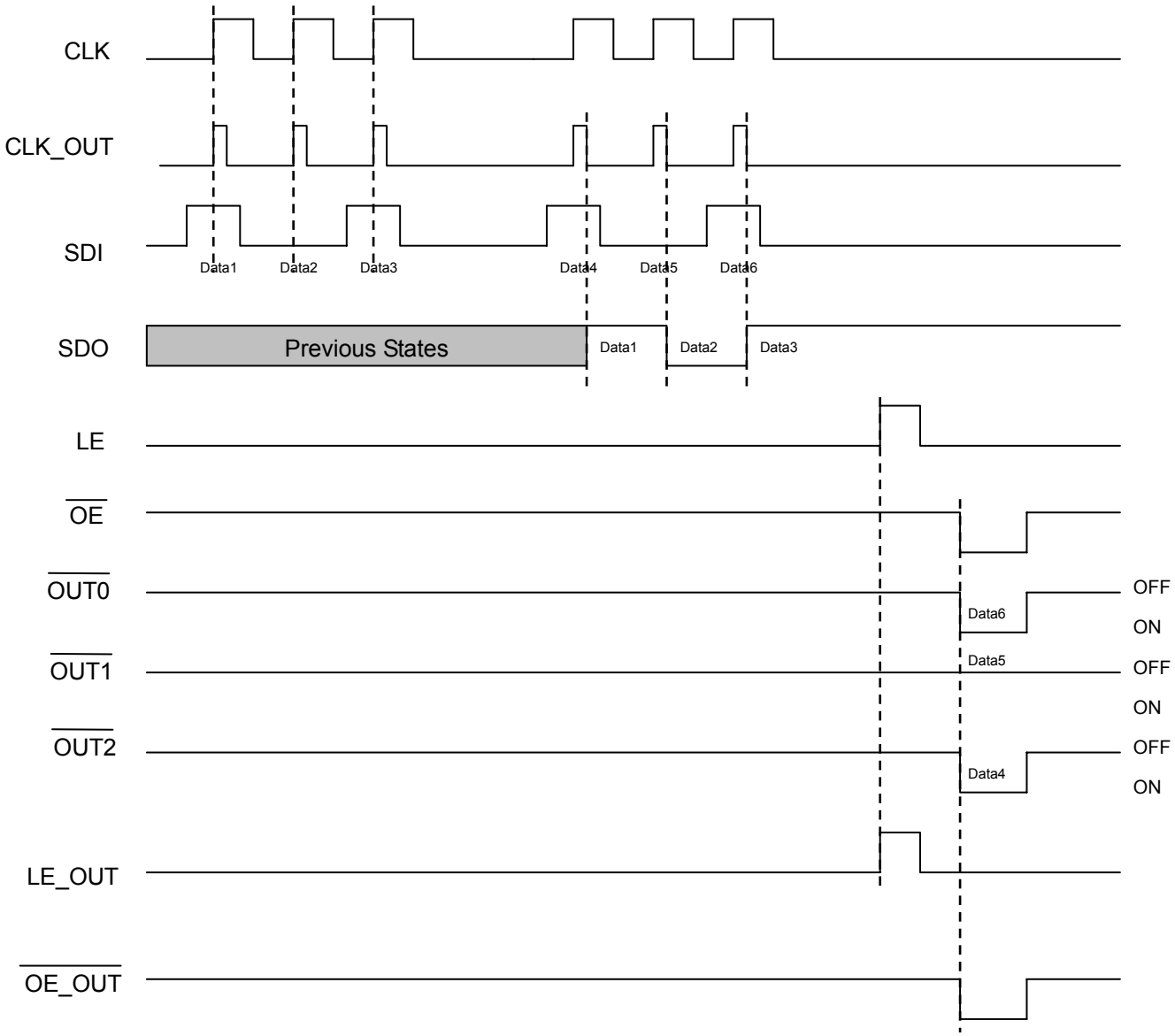
CLK, SDI terminals



SDO, $\overline{OE}\_OUT$, LE_OUT, CLK_OUT terminals



Timing Diagram



Maximum Ratings

Characteristic	Symbol	Rating	Unit
Supply Voltage	V_{DD}	15	V
Input Voltage	V_{IN}	-0.4~V_{DD}+0.4	V
Output Current per Output Channel	I_{OUT}	+90	mA
Sustaining Voltage at OUT port	V_{DS}	17.0	V
GND Terminal Current	I_{GND}	1000	mA
Power Dissipation at 25°C	P_D	1.7	W
Thermal Resistance	$R_{th(j-a)}$	73.43	°C/W
Operating Junction Temperature	$T_{j,max}$	150	°C
Operating Temperature	T_{opr}	-40~+85	°C
Storage Temperature	T_{stg}	-55~+150	°C

Electrical Characteristics

MBI6010 electrical characteristics are measured under the test conditions where TA=25°C and V_{DD}=6.0~12.0V.

Characteristic		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		6.0	-	12	V
Output Voltage of CA,CB		V_{CA},V_{CB}	When V_{DD}=12V		4.8	5.3	6.0	V
Input Voltage	"H" level	V_{IH}	V_{CB}=5V under I_{OUT}≦0.5μA		3.5	-	12.0	V
	"L" level	V_{IL}	V_{CB}=5V under I_{OUT}≦0.5μA		GND	-	1.4	V
Output Current		I_{OH}	SDO, LE_OUT, $\overline{OE\_OUT}$, CLK_OUT, at V_{OH}=3.5V (refer to Fig. 2)		-	-20	-	mA
		I_{OL}	SDO, LE_OUT, $\overline{OE\_OUT}$, CLK_OUT, at V_{OL}=1.5V (refer to Fig. 2)		-	20	-	mA
Sustaining Voltage		$V_{DS,SUS}$	$\overline{OUT0}$ ~ $\overline{OUT2}$		-	-	17.0	V
Output Leakage Current		$I_{OUT,LEAK}$	V_{DS}=17.0V		-	-	0.5	μA
Voltage at signal output terminals	SDO, LE_OUT, $\overline{OE\_OUT}$, CLK_OUT	V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA (refer to V_{CA}, V_{CB})		4.5	-	-	V
Output Current		I_{OUT}	DC Test Circuit, $\overline{OUT0}$ ~ $\overline{OUT2}$		5	-	60	mA
Output Current 1		I_{OUT1}	V_{DS}=0.8V	R_{ext}=6KΩ	-	26.0	-	mA
Current Skew 1		dI_{OUT1}	I_{OL}=25.0mA V_{DS}=0.8V	R_{ext}=6KΩ	-	-	±6	%
Output Current 2		I_{OUT2}	V_{DS}=0.8V	R_{ext}=30KΩ	-	5.0	-	mA
Current Skew 2		dI_{OUT2}	I_{OL}=5.0mA V_{DS}=0.8V	R_{ext}=30KΩ	-	-	±6	%
Regulation of Output Current vs. Voltage at Output Ports		$\%/dV_{DS}$	When V_{DS} is within 1.0V and 3.0V		-	±0.2	-	% / V
Regulation of Output Current vs. Supply Voltage Change		$\%/dV_{DD}$	When V_{DD} is within 6.0V and 12.0V		-	±1.0	-	% / V
Voltage at R-EXT0, R-EXT1, R-EXT2 pins		V_{REXT}	When V_{DD} is within 6.0V and 12.0V		1.2	1.24	1.3	V
Pull-up Resistor		R_{IN}(up)	$\overline{OE}$, R_{IN}(up)= R_{IN1}(up)+ R_{IN2}(up)		400	700	1000	KΩ
Pull-down Resistor		R_{IN}(down)	LE , R_{IN}(down)= R_{IN1}(down)+ R_{IN2}(down)		400	700	1000	KΩ
Supply Current	"OFF"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT2}$ =Off		-	4	7	mA
		I_{DD}(off) 2	R_{ext}=6KΩ, $\overline{OUT0}$ ~ $\overline{OUT2}$ =Off		-	5	8	
		I_{DD}(off) 3	R_{ext}=30KΩ, $\overline{OUT0}$ ~ $\overline{OUT2}$ =Off		-	7	10	
	"ON"	I_{DD}(on) 1	R_{ext}=6KΩ, $\overline{OUT0}$ ~ $\overline{OUT2}$ =On		-	5	8	
		I_{DD}(on) 2	R_{ext}=30KΩ, $\overline{OUT0}$ ~ $\overline{OUT2}$ =On		-	7	10	

Test Circuit for Electrical Characteristics

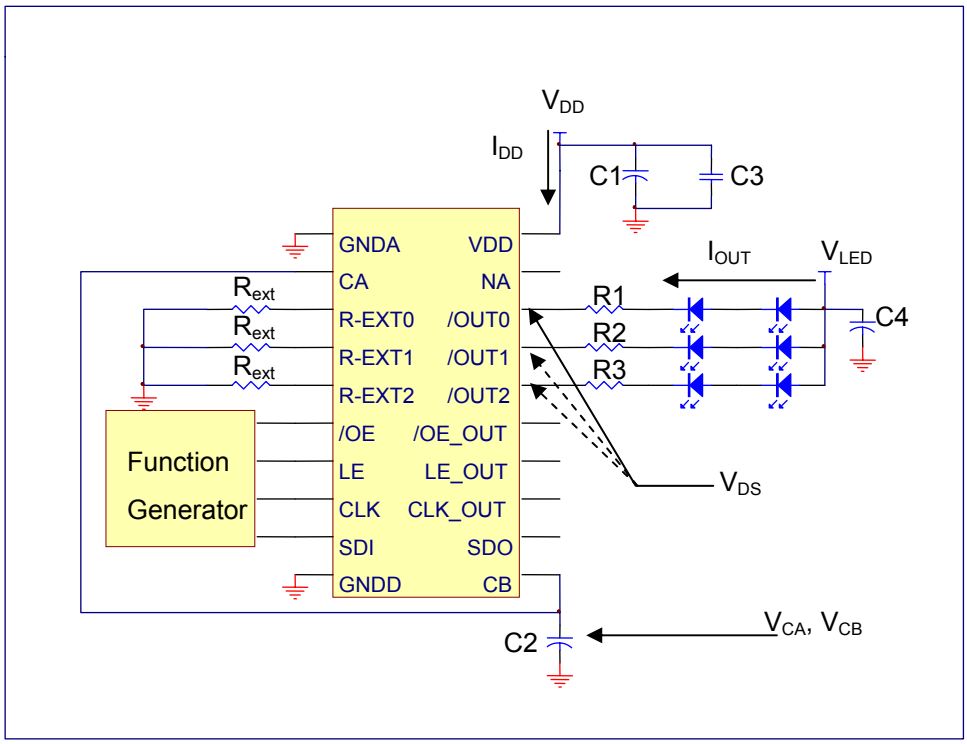


Figure 1

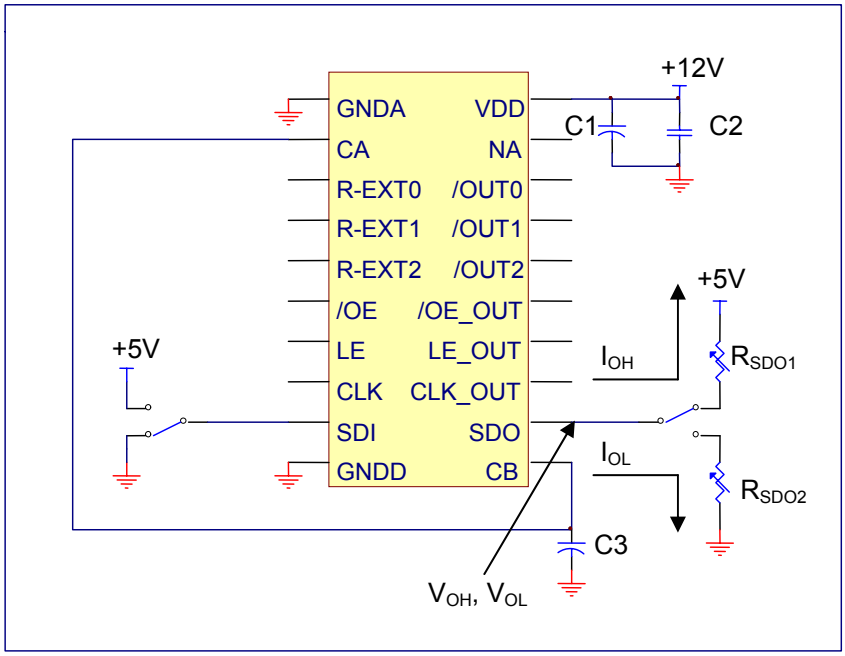


Figure 2

Switching Characteristics

Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit
Delay time ("L" to "H")	$\overline{OE}$ - $\overline{OE\_OUT}$ LE-LE_OUT CLK-CLK_OUT	t_{pLH1}	T_A=25°C V_{DD}=12V V_{DS}=1V V_{IH}=VDD V_{IL}=GND R_{ext}=7.5KΩ (I_{OUT}=20mA) V_L=5V R_L=150Ω C_L=10pF	-	20	30	ns
	$\overline{OE\_OUT_0}$	t_{pLH2}		-	100	150	ns
Delay Time ("H" to "L")	$\overline{OE}$ - $\overline{OE\_OUT}$ LE-LE_OUT	t_{pHL1}		-	20	30	ns
	$\overline{OE\_OUT_0}$	t_{pHL2}		-	100	150	ns
	CLK_OUT-SDO	t_{pHL3}		-	5	20	ns
Pulse Width	CLK_OUT	$t_{w(CLK\_OUT)}$		30	40	50	ns
Stagger Delay Time	Output Ports	t_S		-	80	-	ns
Rise Time	$\overline{OE\_OUT}$	$t_{r(OE)}$		-	3	10	ns
	LE_OUT	$t_{r(LE)}$		-	3	10	ns
	CLK_OUT	$t_{r(CLK)}$		-	5	10	ns
	SDO	$t_{r(SDO)}$		-	5	10	ns
	Output Ports	t_{or}		-	180	220	ns
Fall Time	$\overline{OE\_OUT}$	$t_{f(OE)}$		-	3	10	ns
	LE_OUT	$t_{f(LE)}$		-	3	10	ns
	CLK_OUT	$t_{f(CLK)}$		-	5	10	ns
	SDO	$t_{f(SDO)}$		-	5	10	ns
	Output Ports	t_{of}		-	60	100	ns
Hold Time	LE	$t_{h(L)}$		5	-	-	ns
	SDI	$t_{h(D)}$		10	-	-	ns
Setup Time	LE	$t_{su(L)}$		25	-	-	ns
	SDI	$t_{su(D)}$		5	-	-	ns
Pulse Width	$\overline{OE}$	$t_{w(OE)}$		5*	-	-	μs
	LE	$t_{w(L)}$		50	-	-	ns
	CLK	$t_{w(CLK)}$		30	-	-	ns
Frequency	CLK	F_{CLK}		-	-	5	MHz
Maximum CLK Rise Time		t_r		-	-	500	ns
Maximum CLK Fall Time		t_f		-	-	500	ns

*When $\overline{OE}$ > 5μs, the deviation of the turn-on time of OUT0, OUT1, OUT2 is negligible.

Test Circuit for Switching Characteristics

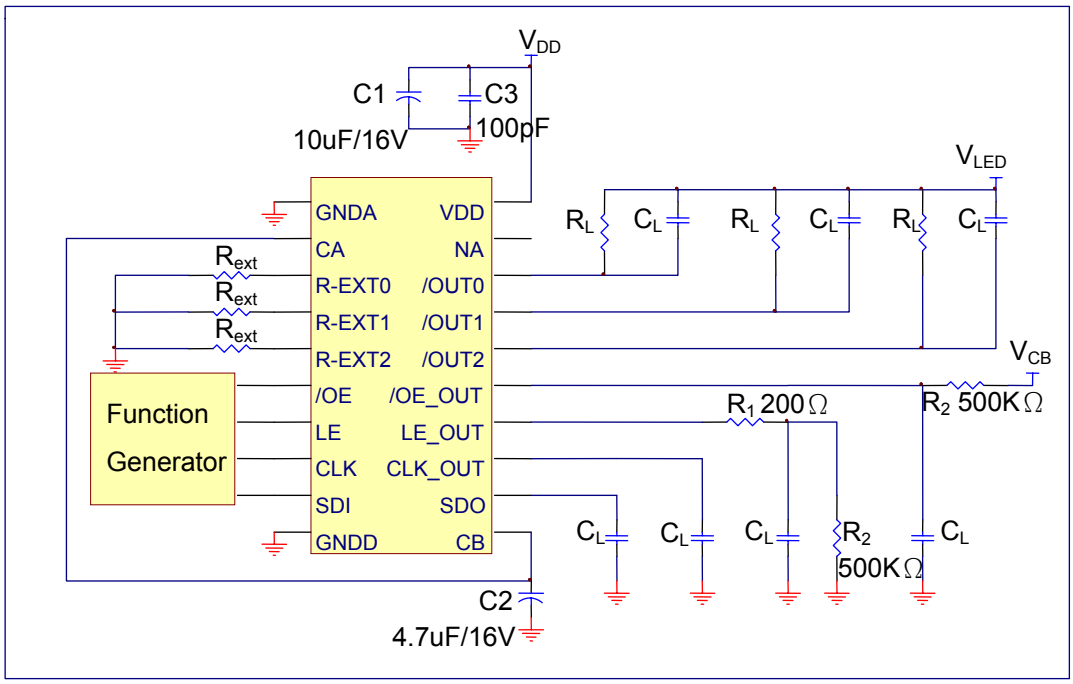
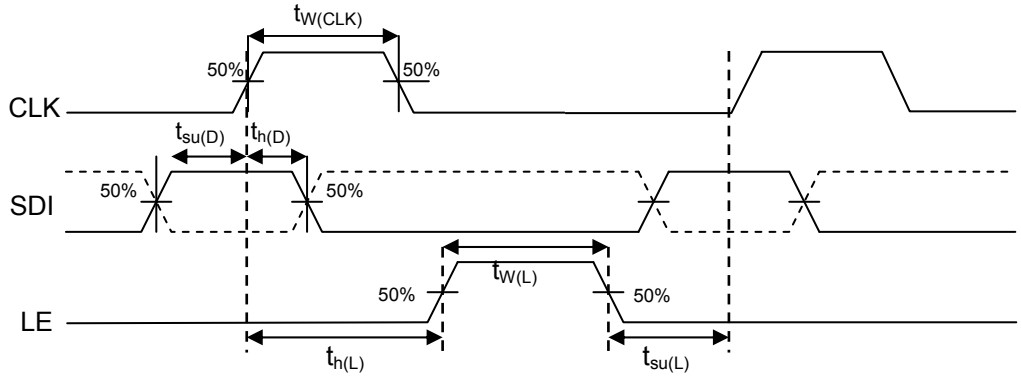
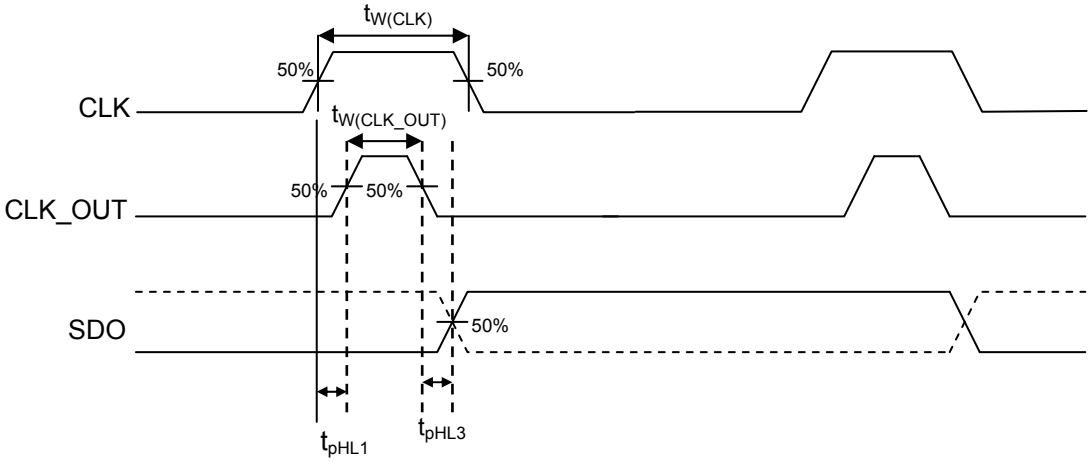
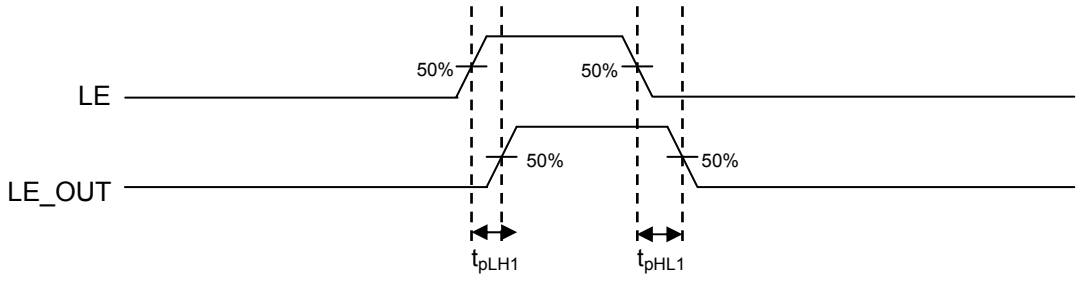


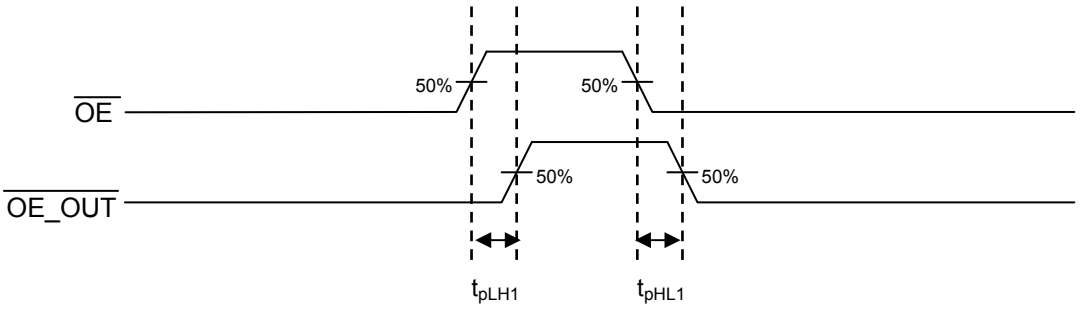
Figure 3

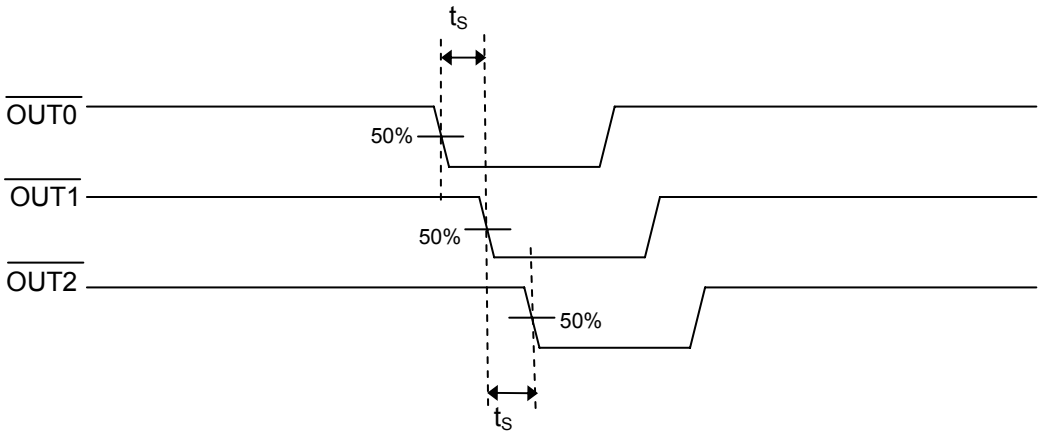
Timing Waveform








OE
OE_OUT
50%
50%
50%
50%
tpLH1
tpHL1


tS
OUT0
OUT1
OUT2
50%
50%
50%
tS

Application Information

Application Circuit*

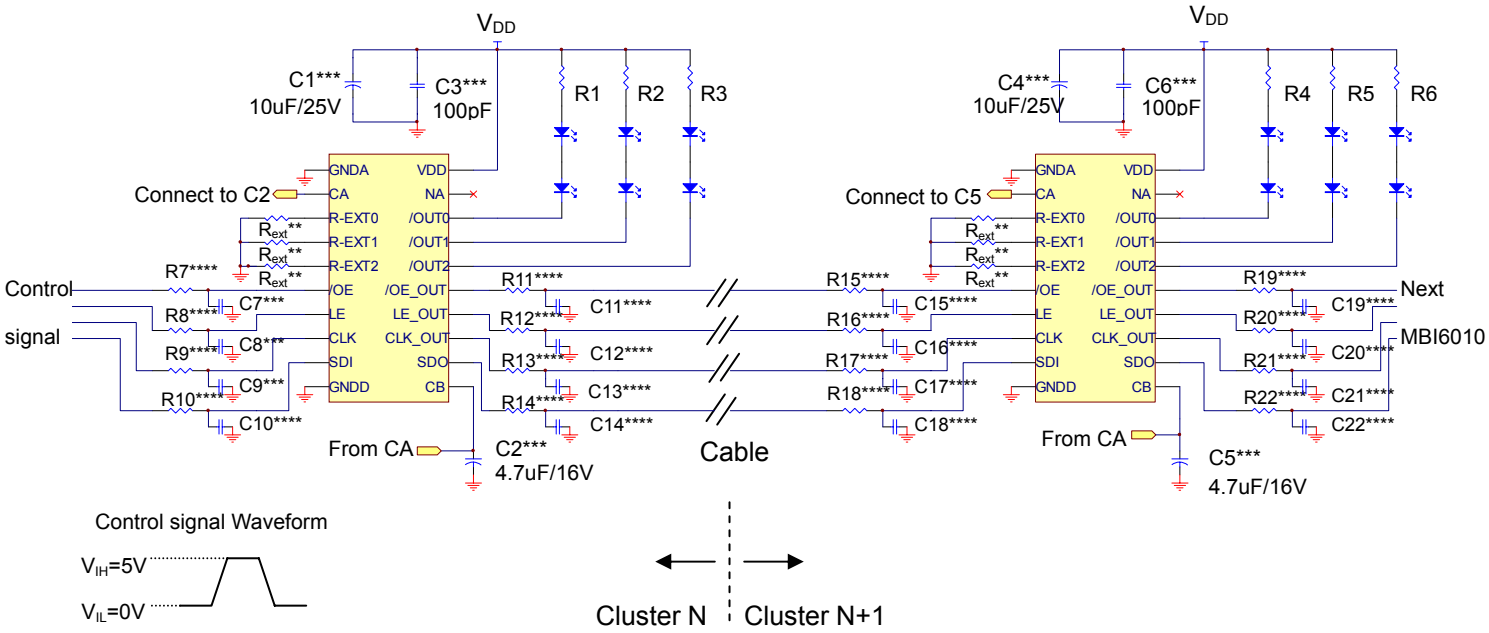


Figure 4

* For detailed circuit information, please refer to the MBI6010 Application Note.

** When the R_{ext} is 7.5kΩ, the I_{OUT} is 20mA.

***C1~C6 are required. The values of the C1/C4 and C3/C6 are for reference only. The value of C2/C5 ranges from 4.7uF/16V to 10uF/16V. Tantalum capacitors or capacitors with ESR < 2Ω are recommended.

****C7~C22 and R7~R22 can modify the signal waveforms. For detailed information, please refer to the MBI6010 Application Note.

Constant Current

In LED display application, MBI6010 provides nearly no variation in current from channel to channel and from IC to IC. This can be achieved by:

1) The maximum current variation between channels is less than ±5%, and that between ICs is less than ±5%.

2) In addition, the current characteristic of output stage is flat and users can refer to the figure as shown below. The output current can be kept constant regardless of the variations of LED forward voltages (V_F). This guarantees LED to be performed on the same brightness as user's specification.

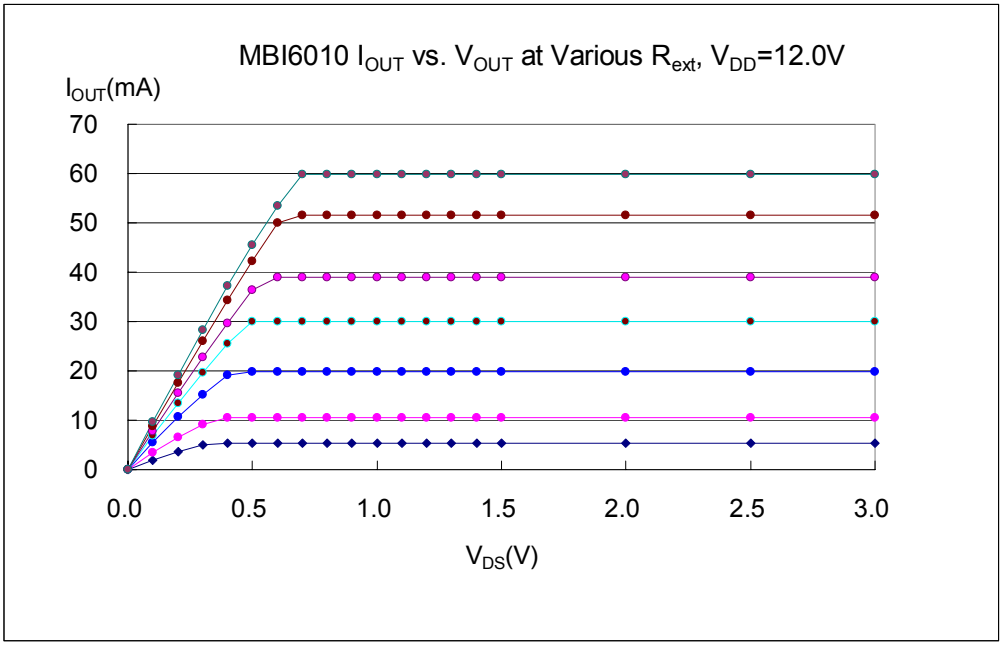


Figure 5

Setting Output Current

The output current of each channel (I_{OUT}) is set by an external resistor, R_{ext}. The relationship between I_{OUT} and R_{ext} is shown in the following figure.

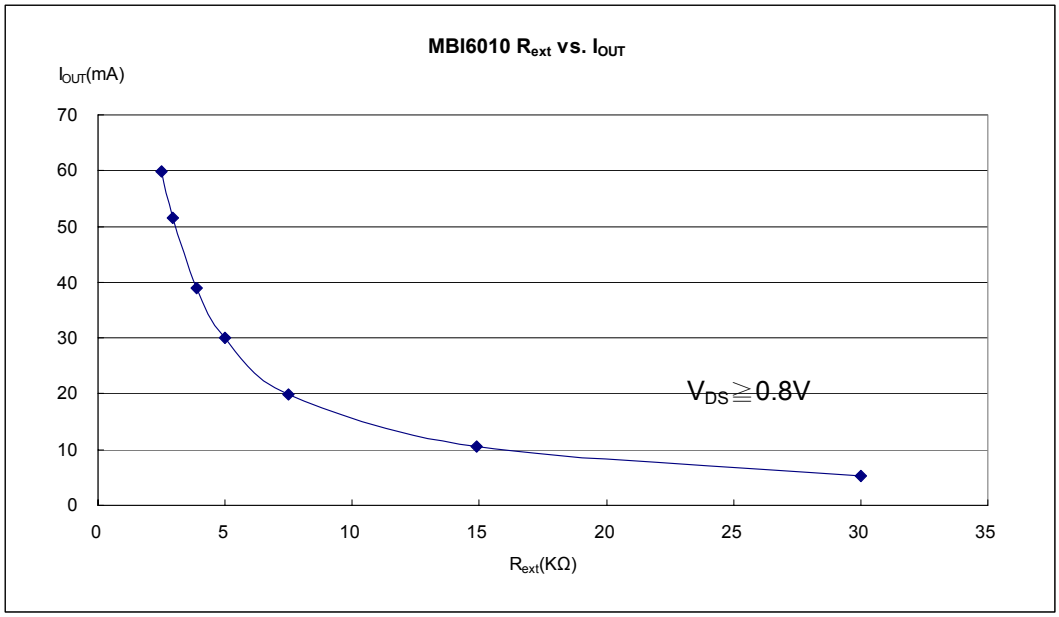


Figure 6

Also, the output current can be calculated from the equation:

$I_{OUT}=V_{REXT} / R_{ext} *120;$

$V_{REXT}= 1.24V;$

where R_{ext} is the resistance of the external resistor connected to R-EXT terminal. The magnitude of current (as a function of R_{ext}) is around 60mA at 2.5KΩ and 20mA at 7.5KΩ.

Package Power Dissipation (P_D)

The maximum power dissipation, $P_D(max)=(T_{j,max} – T_a) / R_{th(j-a)}$, decreases as the ambient temperature increases.

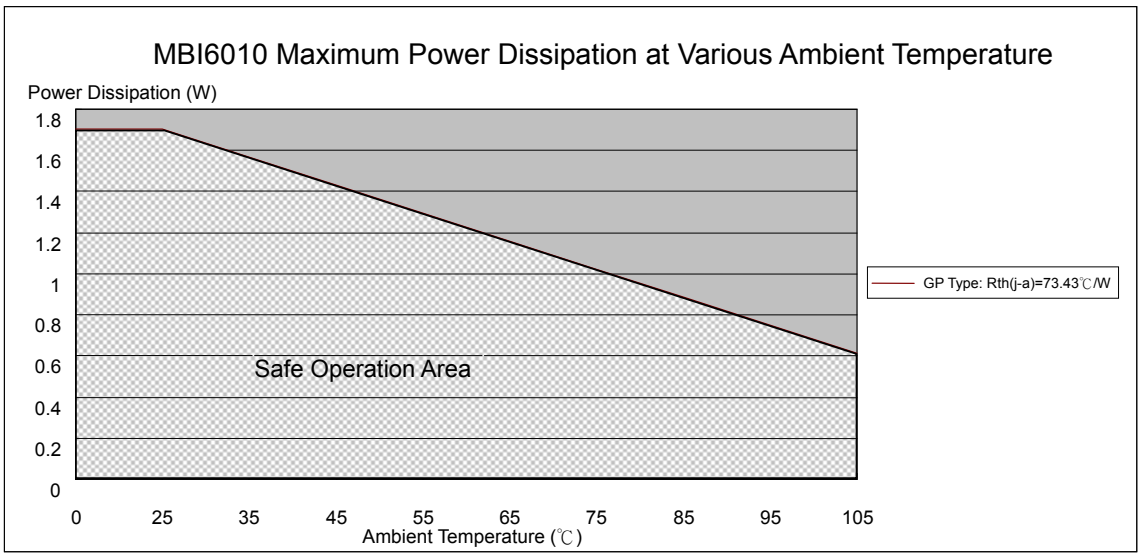


Figure 7

Load Supply Voltage (V_{LED})

MBI6010 is designed to operate with adequate V_{DS} to achieve constant current. V_{DS} together with I_{OUT} should not exceed the package power dissipation limit, $P_{D(max)}$.

As in Figure 8, $V_{DS} = V_{LED} – V_F$, and V_{LED} is the load supply voltage. $P_{D(act)}$ will be greater than $P_{D(max)}$, if V_{DS} drops too much voltage on the driver. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer, V_{DROP}.

A voltage reducer lets $V_{DS} = (V_{LED} –V_F) – V_{DROP}$.

Resistors can be used in the applications as shown in Figure 8.

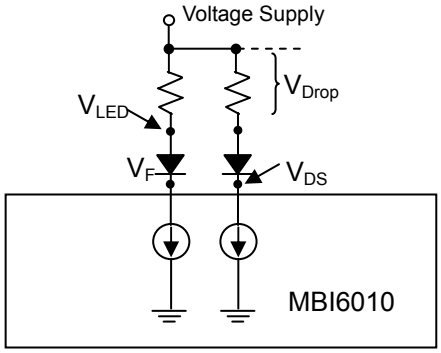
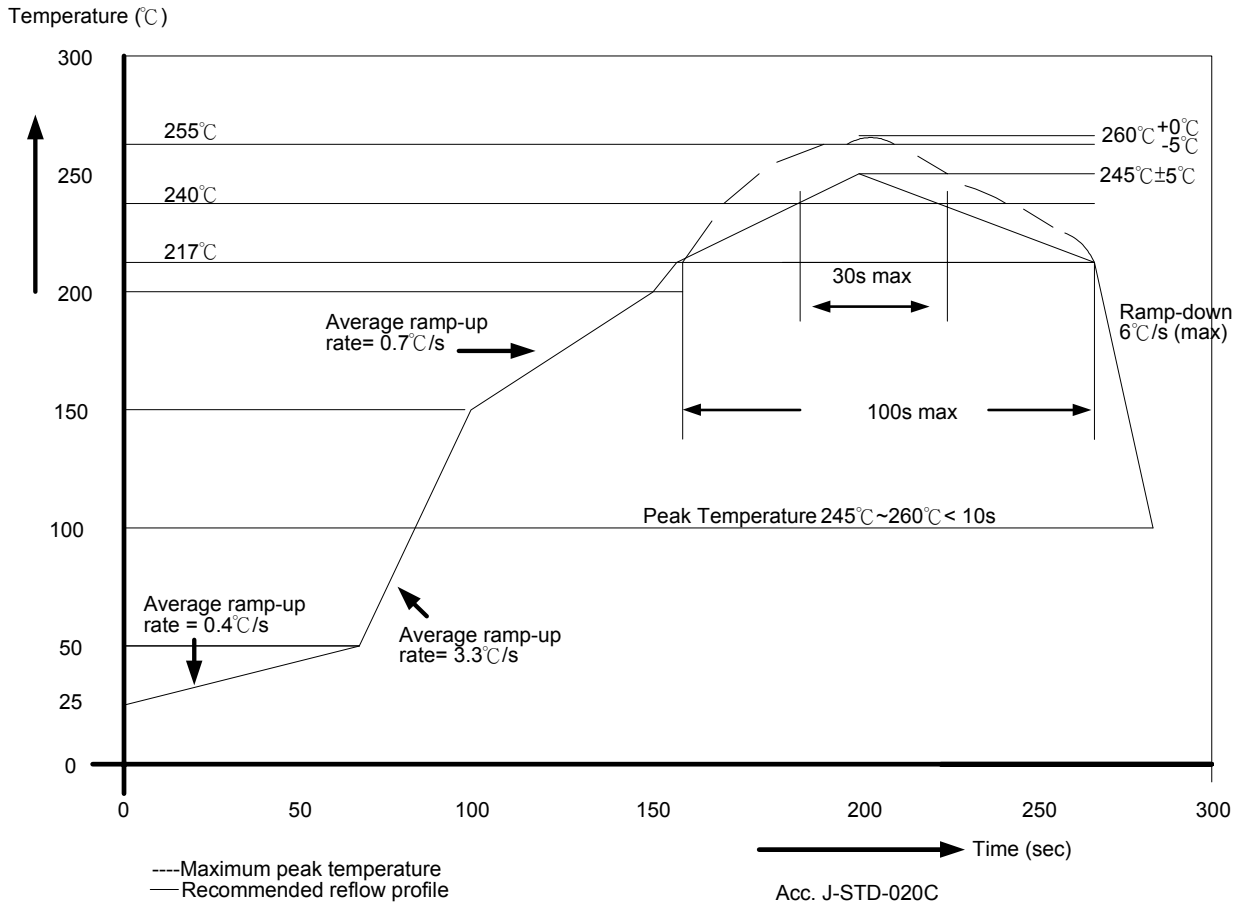


Figure 8

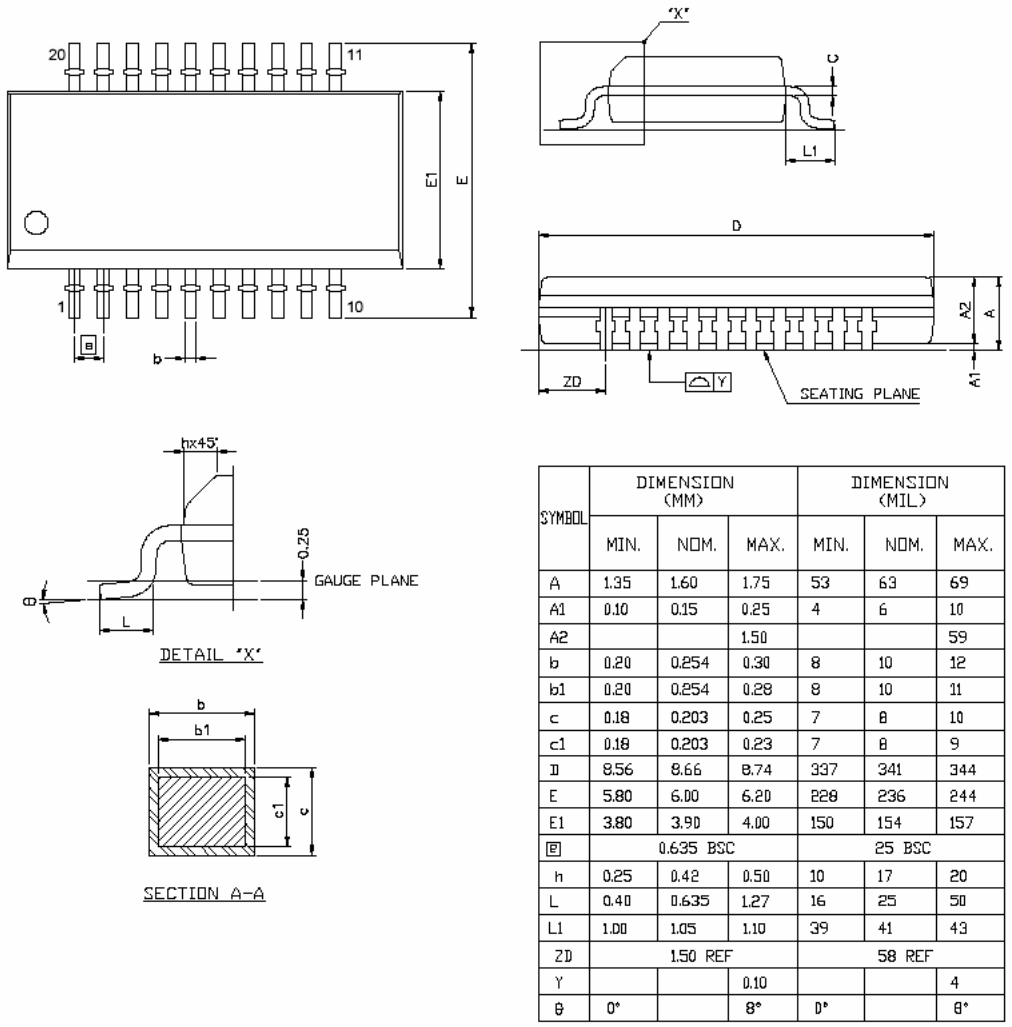
Soldering Process of “Pb-free & Green” Package Plating*

Macroblock has defined "Pb-Free & Green" to mean semiconductor products that are compatible with the current RoHS requirements and selected 100% pure tin (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it is backward compatible to standard 215ºC to 240ºC reflow processes which adopt tin/lead (SnPb) solder paste. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn) will all require up to 260°C for proper soldering on boards, referring to J-STD-020C as shown below.



*Note: For details, please refer to Macroblock’s “Policy on Pb-free & Green Package”.

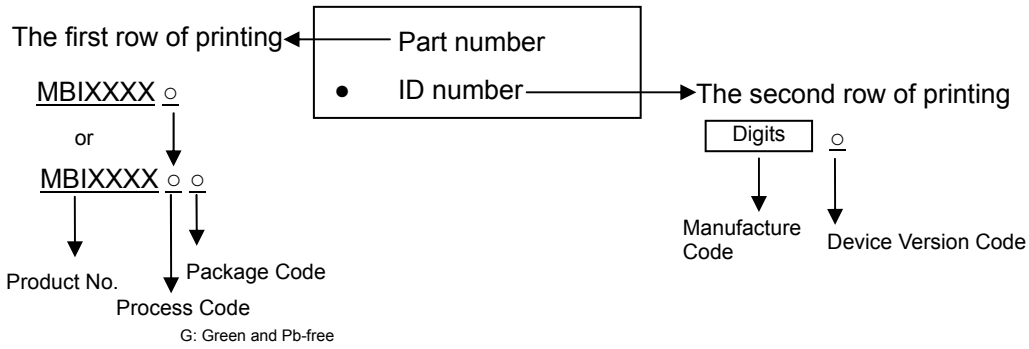
Package Outline



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.60	1.75	53	63	69
A1	0.10	0.15	0.25	4	6	10
A2			1.50			59
b	0.20	0.254	0.30	8	10	12
b1	0.20	0.254	0.28	8	10	11
c	0.18	0.203	0.25	7	8	10
c1	0.18	0.203	0.23	7	8	9
D	8.56	8.66	8.74	337	341	344
E	5.80	6.00	6.20	228	236	244
E1	3.80	3.90	4.00	150	154	157
e	0.635 BSC			25 BSC		
h	0.25	0.42	0.50	10	17	20
L	0.40	0.635	1.27	16	25	50
L1	1.00	1.05	1.10	39	41	43
ZD	1.50 REF			58 REF		
Y			0.10			4
θ	0°		8°	0°		8°

MBI6010GP Outline Drawing

Product Top-mark Information



Product Revision History

Datasheet Version	Device Version Code
V1.00	A

Product Ordering Information

Part Number	Package Type	Weight (g)	Minimum Order Quantity (Pieces per Reel)
MBI6010GP	SSOP20-150-0.65	0.635	-